
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(Case No.: RA001C14)

In the Application of:)
)
FARMWALD ET AL.)
)
Serial No: Continuation of 09/969,489)
)
Filed: Herewith)
)
Title: SYNCHRONOUS MEMORY DEVICE HAVING)
AUTOMATIC PRECHARGE (As Amended))

Assistant Commissioner for Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Dear Sir:

Prior to the examination of the above-referenced application, kindly amend the application as follows:

IN THE ABSTRACT:

Please delete the Abstract of the Disclosure and substitute the attached Abstract of the Disclosure.

IN THE TITLE:

Please delete the title and substitute:

SYNCHRONOUS MEMORY DEVICE HAVING AUTOMATIC PRECHARGE

IN THE SPECIFICATION:

(A marked-up version of the following amendments to the Specification is enclosed herewith)

On page 1, line 8, **insert**:

This application is a continuation of Application No. 09/969,489, (still pending) which is a continuation of Application No. 09/669,295, filed on September 25, 2000 (now U.S. Patent 6,304,937), which is a continuation of Application No. 09/510,213, filed on February 22, 2000 (now U.S. Patent 6,182,184) which is a continuation of Application No. 09/252,998, filed on February 19, 1999 (now U.S. Patent 6,032,214), which is a continuation of Application No. 08/979,127, filed on November 26, 1997 (now U.S. Patent 5,915,105), which is a continuation of Application No. 08/762,139, filed on December 9, 1996 (now U.S. Patent 5,809,263); which is a continuation of Application No. 08/607,780, filed February 27, 1996 (now abandoned); which is a continuation of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).

On page 3, **substitute** the paragraph starting on line 6 with the following paragraph:

Prior art memory systems have attempted to solve the problem of high speed access to memory with limited success. U.S. Pat. No. 3,821,715 (Hoff et.al.), was issued to Intel Corporation for the earliest 4-bit microprocessor. That patent describes a bus connecting a single central processing unit (CPU) with multiple RAMs and ROMs. That bus multiplexes addresses and data over a 4-bit wide bus and uses point-to-point control signals to select particular RAMs or ROMs. The access time is fixed and only a single processing element is permitted. There is no block-mode type of operation, and most important, not all of the interface signals between the devices are bused (the ROM and RAM control lines and the RAM select lines are point-to-point).

On page 6, **substitute** the paragraph starting on line 1, with the following paragraph:

In U.S. Pat. No. 4,646,270 (Voss), a video RAM is described which implements a parallel-load, serial-out shift register on the output of a DRAM. This generally allows greatly improved bandwidth (and has been extended to 2, 4 and greater width shift-out paths.) The rest of the interfaces to the DRAM (RAS, CAS, multiplexed address, etc.) remain the same as for conventional DRAMS.

On page 10, **substitute** the paragraphs starting on lines 18 and 21 , with the following two paragraphs, respectively:

FIGS. 7a and 7b show the timing whereby signals from two devices can overlap temporarily and drive the bus at the same time.

FIGS. 8a and 8b show the connection and timing between bus clocks and devices on the bus.

On page 34, **substitute** the paragraph starting on line 4, with the following paragraph:

Slave devices do not need to detect a collision directly, but they must wait to do anything irrecoverable until the last byte (byte 5) is read to ensure that the packet is valid. A request packet with Master[0:3] equal to 0 (a retry signal) is ignored and does not cause a collision. The subsequent bytes of such a packet are ignored.

Please **substitute** the paragraph starting on page 40, line 19, and ending on page 41, line 16, with the following paragraph:

In a preferred embodiment, a standard data block size can be selected for use with ECC, and the ECC method will determine the required number of bits of information in a corresponding ECC block. RAMs containing ECC information can be programmed to store an access time that is equal to: (1) the access time of the normal RAM (containing data) plus the time to access a standard data block (for corrected data) minus the time to send a request packet (6 bytes); or (2) the access time of a normal RAM minus the time to access a standard ECC block minus the time to send a

request packet. To read a data block and the corresponding ECC block, the master simply issues a request for the data immediately followed by a request for the ECC block. The ECC RAM will wait for the selected access time then drive its data onto the bus right after (in case (1) above)) the data RAM has finished driving out the data block. Persons skilled in the art will recognize that the access time described in case (2) above can be used to drive ECC data before the data is driven onto the bus lines and will recognize that writing data can be done by analogy with the method described for a read. Persons skilled in the art will also recognize the adjustments that must be made in the bus-busy structure and the request packet arbitration methods of this invention in order to accommodate these paired ECC requests.

Please **substitute** the paragraph starting on page 45, line 17, and ending on page 46, line 17, with the following:

Referring to FIGS. 7a and 7b, although there is no stable condition where two devices drive the bus at the same time, conditions can arise because of propagation delay on the wires where one device, A 41, can start driving its part of the bus 44 while the bus is still being driven by another device, B 42 (already asserting a logical 1 on the bus). In a system using current drivers, when B 42 is driving the bus (before time 46), the value at points 44 and 45 is logical 1. If B 42 switches off at time 46 just when A 41 switches on, the additional drive by device A 41 causes the voltage at the output 44 of A 41 to briefly below the normal value. The voltage returns to its normal value at time 47 when the effect of device B 42 turning off is felt. The voltage at point 45 goes to logical 0 when device B 42 turns off, then drops at time 47 when the effect of device A 41 turning on is felt. Since the logical 1 driven by current from device A 41 is propagated irrespective of the previous value on the bus, the value on the bus is guaranteed to settle after one time of flight (t_f) delay, that is, the time it takes a signal to propagate from one end of the bus to the other. If a voltage drive was used (as in ECL wired-ORing), a logical 1 on the bus (from device B 42 being previously driven) would prevent the transition put out by device A 41 being felt at the most remote part of the system, e.g., device 43, until the turnoff waveform from device B 42 reached device A 41 plus one time of flight delay, giving a worst case settling time of twice the time of flight delay.

Please **substitute** the paragraph starting on page 46, line 20, and ending on page 47, line 12, with the following paragraph:

Clocking a high speed bus accurately without introducing error due to propagation delays can be implemented by having each device monitor two bus clock signals and then derive internally a device clock, the true system clock. The bus clock information can be sent on one or two lines to provide a mechanism for each bused device to generate an internal device clock with zero skew relative to all the other device clocks. Referring to FIG. 8a, in the preferred implementation, a bus clock generator 50 at one end of the bus propagates an early bus clock signal in one direction along the bus, for example on line 53 from right to left, to the far end of the bus. The same clock signal then is passed through the direct connection shown to a second line 54, and returns as a late bus clock signal along the bus from the far and to the origin, propagating from left to right. A single bus clock line can be used if it is left unterminated at the far end of the bus, allowing the early bus clock signal to reflect back along the same line as a late bus clock signal.

video controllers or I/O devices can also be attached to either the transceiver bus or a primary bus unit, as desired. Persons skilled in the art will recognize how to use a single primary bus unit or multiple primary bus units as needed with a transceiver bus in certain system designs.

Please **substitute** the paragraph starting on page 53, line 24, and ending on page 54, line 22, with the following paragraph:

A block diagram of the preferred input/output circuit for address/data/control lines is shown in FIG. 10. This circuitry is particularly well-suited for use in DRAM devices but it can be used or modified by one skilled in the art for use in other devices connected to the bus of this invention. It consists of a set of input receivers 71, 72 and output driver 76 connected to input/output line 69 and pad 75 and circuitry to use the internal clock 73 and internal clock complement 74 to drive the input interface. The clocked input receivers take advantage of the synchronous nature of the bus. To further reduce the performance requirements for device input receivers, each device pin, and thus each bus line, is connected to two clocked receivers, one to sample the even cycle inputs, the other to sample the odd cycle inputs. By thus de-multiplexing the input 69 at the pin, each clocked amplifier is given a full 2 ns cycle to amplify the bus low-voltage-swing signal into a full value CMOS logic signal. Persons skilled in the art will recognize that additional clocked input receivers can be used within the teachings of this invention. For example, four input receivers could be connected to each device pin and clocked by a modified internal device clock to transfer sequential bits from the bus to internal device circuits, allowing still higher external bus speeds or still longer settling times to amplify the bus low-voltage-swing signal into a full value CMOS logic signal.

Please **substitute** the paragraph starting on page 58, line 13, and ending on 59, line 2, with the following paragraph:

In the preferred embodiment, two sets of these delay lines are used, one to generate the true value of the internal device clock 73, and the other to generate the complement 74 without adding any inverter delay. The dual circuit allows generation of

truly complementary clocks, with extremely small skew. The complement internal device clock is used to clock the `event` input receivers to sample at time 127, while the true internal device clock is used to clock the `odd` input receivers to sample at time 125. The true and complement internal device clocks 73 and 74 are also used to select which data is driven to the output drivers. The gate delay between the internal device clock and output circuits driving the bus is slightly greater than the corresponding delay for the input circuits, which means that the new data always will be driven on the bus slightly after the old data has been sampled.

Please substitute the paragraph starting on page 60, line 1, and ending on page 61, line 8, with the following paragraph:

Running the internal I/O lines in the conventional way at high bus cycle rates is not possible. In the preferred method, several (preferably 4) bytes are read or written during each cycle and the column access path is modified to run at a lower rate (the inverse of the number of bytes accessed per cycle, preferably 1/4 of the bus cycle rate). Three different techniques are used to provide the additional internal I/O lines required and to supply data to memory cells at this rate. First, the number of I/O bit lines in each subarray running through the column decoder 147 A, B is increased, for example, to 16, eight for each of the two columns of column sense amps and the column decoder selects one set of columns from the "top" half 148 of subarray 150 and one set of columns from the "bottom" half 149 during each cycle, where the column decoder selects one column sense amp per I/O bit line. Second, each column I/O line is divided into two halves, carrying data independently over separate internal I/O lines from the left half 147A and right half 147B of each subarray (dividing each subarray into quadrants) and the column decoder selects sense amps from each right and left half of the subarray, doubling the number of bits available at each cycle. Thus each column decode selection turns on n column sense amps, where n equals four (top left and right, bottom left and right quadrants) times the number of I/O lines in the bus to each subarray quadrant (8 lines each times 4=32 lines in the preferred implementation). Finally, during each RAS cycle, two different subarrays, e.g. 157 and 153, are accessed. This doubles again the available number of I/O lines containing data. Taken

together, these changes increase the internal I/O bandwidth by at least a factor of 8. Four internal buses are used to route these internal I/O lines. Increasing the number of I/O lines and then splitting them in the middle greatly reduces the capacitance of each internal I/O line which in turn reduces the column access time, increasing the column access bandwidth even further.

IN THE CLAIMS:

Kindly **cancel** claims 1-150, without prejudice.

Kindly **add** the following claims:

1 151. (New) A synchronous integrated circuit device having a memory array which
2 includes dynamic random access memory cells, wherein the integrated circuit device
3 comprises:

4 a clock receiver to receive an external clock signal;

5 a plurality of sense amplifiers, coupled to the memory array, to sense data from
6 the dynamic random access memory cells; and

7 a plurality of input receivers to sample an operation code synchronously with
8 respect to a transition of the external clock signal, the operation code including
9 precharge information, wherein, in response to the precharge information, the plurality
10 of sense amplifiers is automatically precharged after the data is sensed.

1 152. (New) The integrated circuit device of claim 151 wherein the operation code
2 specifies a read operation, and wherein the integrated circuit device further includes a
3 plurality of output drivers to output first and second portions of the data in response to
4 the operation code specifying a read operation.

1 153. (New) The integrated circuit device of claim 152 wherein:

2 the plurality of output drivers output the first portion of the data synchronously
3 with respect to a rising edge transition of the external clock signal; and

4 the plurality of output drivers output a second portion of the data synchronously
5 with respect to a falling edge transition of the external clock signal.

1 154. (New) The integrated circuit device of claim 153 further including a delay
2 lock loop, coupled to the plurality of output drivers, to synchronize the output of the first
3 and second portions of the data with the external clock signal.

1 155. (New) The integrated circuit device of claim 153 further including a plurality
2 of multiplexers, wherein each multiplexer of the plurality of multiplexers is coupled to an
3 output driver of the plurality of output drivers.

1 156. (New) The integrated circuit device of claim 155 wherein:
2 the plurality of multiplexers provide the first portion of the data to the plurality of
3 output drivers in response to a rising transition of the external clock signal; and
4 the plurality of multiplexers provide the second portion of the data to the plurality
5 of output drivers in response to a falling edge transition of the external clock signal.

1 157. (New) The integrated circuit device of claim 151 wherein the plurality of
2 input receivers further includes a first input receiver to sample a first bit of the operation
3 code synchronously with respect to the transition of the external clock signal, wherein
4 the precharge information is encoded in the first bit of the operation code.

1 158. (New) The integrated circuit device of claim 157 wherein the plurality of
2 input receivers further includes a second input receiver to sample a second bit of the
3 operation code synchronously with respect to the transition of the external clock signal,
4 wherein the second bit of the operation code specifies a read operation, wherein a
5 portion of the data is output from the integrated circuit device in response to the second
6 bit of the operation code specifying the read operation.

166. (New) A synchronous integrated circuit memory device including an array of memory cells, wherein the memory device comprises:

a clock receiver to receive an external clock signal;

a plurality of sense amplifiers, coupled to the array of memory cells, to sense

wherein a portion of the data is output from the memory device in response to a

operation code bit specifying a read operation;

a first input receiver to sample the first operation code bit in response to a first edge of the external clock signal;

a second input receiver to sample a second operation code bit in response to the transition of the external clock signal, wherein the second operation code bit indicates whether precharging the plurality of sense amplifiers occurs automatically after data has been sensed; and

a plurality of output drivers to output the portion of the data synchronously with the external clock signal.

167. (New) The memory device of claim 166 wherein the second input receiver samples an address bit synchronously with respect to a second transition of the global clock signal.

168. (New) The memory device of claim 166 wherein the plurality of output
s output the portion of the data onto an external bus, the external bus including a
y of external signal lines.

1 169. (New) The memory device of claim 168 wherein:
2 the first operation code bit is sampled from a first signal line of the plurality of
3 external signal lines; and
4 the second operation code bit is sampled from a second signal line of the
5 plurality of external signal lines.

1 170. (New) The memory device of claim 169 wherein the plurality of external
2 signal lines is used to carry, in a multiplexed format, address information and the portion
3 of the data.

1 171. (New) The memory device of claim 166 further including a delay locked
2 loop, coupled to the clock receiver, to generate an internal clock signal using the
3 external clock signal, wherein the plurality of output drivers output the portion of the data
4 in response to the internal clock signal.

1 172. (New) The memory device of claim 166 further including:
2 row decoder circuitry, coupled to the array of memory cells, to identify a row of
3 the array of memory cells that stores the data to be sensed by the plurality of sense
4 amplifiers; and
5 column decoder circuitry, coupled to the array of memory cells, to identify the
6 portion of the data.

1 177. (New) The method of claim 176 wherein the data is output onto the plurality
2 of signal lines.

1 178. (New) The method of claim 173 further including:
2 selecting a row of memory cell locations in accordance with a first address
3 portion; and
4 sensing data, from the selected row of memory cell locations, in a row of sense
5 amplifiers, wherein the plurality of sense amplifiers is included in the row of sense
6 amplifiers.

1 179. (New) The method of claim 178 further including identifying the plurality of
2 sense amplifiers based on a second address portion.

1 180. (New) The method of claim 173 further including generating an internal
2 clock signal using a delay locked loop, wherein the data is output in response to the
3 internal clock signal.

1 181. (New) The method of claim 173 wherein a first portion of the data is output
2 synchronously with respect to a rising edge transition of the external clock signal, and a
3 second portion of the data is output synchronously with respect to a falling edge
4 transition of the external clock signal.

1 188. (New) The method of claim 187 wherein the address information and the
2 first operation code are issued to the memory device via an external bus.

1 189. (New) A synchronous memory device having a memory array which
2 includes dynamic memory cells, wherein the memory device comprises:

3 a plurality of sense amplifiers, coupled to the memory array, to sense data from
4 the dynamic memory cells; and

5 a plurality of input receivers to sample an operation code synchronously with
6 respect to a transition of an external clock signal, the operation code including
7 precharge information, wherein, in response to the precharge information, the plurality
8 of sense amplifiers are automatically precharged after the data is sensed;

9 a plurality of output drivers to output first and second portions of the data in
10 response to the operation code specifying a read operation; and

11 a delay locked loop, coupled to the plurality of output drivers, to synchronize the
12 output of the first and second portions of the data with the external clock signal.

1 190. (New) The memory device of claim 189 wherein:

2 the plurality of output drivers output the first portion of the data synchronously
3 with respect to a rising edge transition of the external clock signal; and

4 the plurality of output drivers output the second portion of the data synchronously
5 with respect to a falling edge transition of the external clock signal.

1 191. (New) The memory device of claim 189 further including a plurality of
2 multiplexers, wherein each multiplexer of the plurality of multiplexers is coupled to an
3 output driver of the plurality of output drivers.

1 192. (New) The memory device of claim 191 wherein the plurality of
2 multiplexers provide the first portion of the data to the plurality of output drivers in
3 response to a rising transition of the external clock signal and the plurality of
4 multiplexers provide the second portion of the data to the plurality of output drivers in
5 response to a falling edge transition of the external clock signal

1 193. (New) The memory device of claim 189 wherein the plurality of input
2 receivers further includes a first input receiver to sample a first bit of the operation code
3 synchronously with respect to the transition of the external clock signal, wherein the
4 precharge information is encoded in the first bit of the operation code.

1 194. (New) The memory device of claim 193 wherein the plurality of input
2 receivers further includes a second input receiver to sample a second bit of the
3 operation code synchronously with respect to the transition of the external clock signal,
4 wherein an encoding of the second bit of the operation code specifies the read
5 operation.

1 195. (New) The memory device of claim 189 wherein the delay locked loop
2 includes:

3 a delay line to generate an internal clock signal, wherein the internal clock signal
4 has a delay with respect to the external clock signal; and

5 a comparator to compare the internal clock signal with the external clock signal,
6 wherein the delay of the internal clock signal is adjusted based on the comparison
7 between the internal clock signal and the external clock signal.

REMARKS

This Preliminary Amendment seeks to place this application in condition for allowance. This application is a continuation of Application Serial No. 09/969,489 which is a continuation of Application Serial No. 09/669,295. Application Serial No. 09/969,489 is pending.

REQUEST FOR PRIORITY

Applicants request priority to Application Serial No. 07/510,898, filed April 18, 1990, now abandoned. Applicants request such priority through Application No. 09/969,489, (still pending) which is a continuation of Application No. 09/669,295, filed on September 25, 2000 (now U.S. Patent 6,304,937), which is a continuation of Application No. 09/510,213, filed on February 22, 2000 (now U.S. Patent 6,182,184) which is a continuation of Application No. 09/252,998, filed on February 19, 1999 (now U.S. Patent 6,032,214), which is a continuation of Application No. 08/979,127, filed on November 26, 1997 (now U.S. Patent 5,915,105), which is a continuation of Application No. 08/762,139, filed on December 9, 1996 (now U.S. Patent 5,809,263); which is a continuation of Application No. 08/607,780, filed February 27, 1996 (now abandoned); which is a continuation of Application No. 08/222,646, filed on March 31, 1994 (now U.S. Patent 5,513,327); which is a continuation of Application No. 07/954,945, filed on September 30, 1992 (now U.S. Patent 5,319,755); which is a continuation of Application No. 07/510,898, filed on April 18, 1990 (now abandoned).

Accordingly, Applicants claim the benefit of the filing date of Application Serial No. 07/510,898 -- i.e., April 18, 1990. The specification has been amended to identify the continuation/divisional or related U.S. application data identified above. No new matter has been added.

AMENDMENTS TO THE CLAIMS

In this continuation application, Applicants present new claims which set forth novel and unobvious features of Applicants' invention. Applicants submit new claims 151-195 to more fully protect the Applicants invention. No new matter has been added.

The newly submitted claims are believed to be fully supported by the specification -- see, for example, page 72 lines 4-16; page 74, line 33 to page 75, line 7; page 93, line 19 to page 94, line 6; page 96, line 21 to page 97, line 25; Figures 1, 2, 4 and 10-13, and 15; page 20, line 20 to page 24, line 17; page 25, lines 1-6; page 46, line 23 to page 47, line 1; page 48, lines 6-17; page 53, line 23 to page 59, line 19.

AMENDMENTS TO THE SPECIFICATION

Applicants have also amended the specification to include the priority data, and to correct obvious spelling, typographical and grammatical errors. No new matter has been added.

AMENDMENTS TO THE ABSTRACT

A new Abstract of the Disclosure is attached hereto. No new matter has been added.

DRAWING CHANGES

Applicants seek to amend Figure 10 to more fully reflect the discussion in the specification, in particular, page 55, lines 12-16 and page 58, lines 13-23. The proposed changes are indicated in red. No new matter has been added. Applicants respectfully request that the Examiner approve the proposed changes to Figure 10. A new Figure 10 which incorporates the changes is also attached to the Request.

CONCLUSION

Applicants request entry of the foregoing amendment prior to examination of this application. Applicants submit that all of the claims present patentable subject matter. Accordingly, Applicants respectfully request allowance of all of the claims.

Date: Dec 21/01

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Respectfully submitted,



Jose G. Moniz
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ABSTRACT OF THE DISCLOSURE

A synchronous integrated circuit memory device including an array of memory cells. The memory device includes a clock receiver to receive an external clock signal, and a plurality of sense amplifiers, coupled to the array of memory cells, to sense data. A first portion of the data is output from the memory device in response to a first operation code bit specifying a read operation. In addition, the memory device includes a first input receiver to sample the first operation code bit in response to a first transition of the external clock signal. Furthermore, the memory device includes a second input receiver to sample a second operation code bit in response to the first transition of the external clock signal. The second operation code bit indicates whether precharging the plurality of sense amplifiers occurs automatically after the data has been sensed. Moreover, the memory device includes a plurality of output drivers to output the portion of the data synchronously with respect to the external clock signal.

Version With Markings to show Changes made to the Specification

On page 3, starting on line 6:

Prior art memory systems have attempted to solve the problem of high speed access to memory with limited success. U.S. Pat. No. 3,821,715 (Hoff et.al.), was issued to Intel Corporation for the earliest 4-bit [micro-processor] microprocessor. That patent describes a bus connecting a single central processing unit (CPU) with multiple RAMs and ROMs. That bus multiplexes addresses and data over a 4-bit wide bus and uses point-to-point control signals to select particular RAMs or ROMs. The access time is fixed and only a single processing element is permitted. There is no block-mode type of operation, and most important, not all of the interface signals between the devices are bused (the ROM and RAM control lines and the RAM select lines are point-to-point).

On page 6, starting on line 1:

In U.S. Pat. No. 4,646,270 [4,646,279](Voss), a video RAM is described which implements a parallel-load, serial-out shift register on the output of a DRAM. This generally allows greatly improved bandwidth (and has been extended to 2, 4 and greater width shift-out paths.) The rest of the interfaces to the DRAM (RAS, CAS, multiplexed address, etc.) remain the same as for conventional DRAMS.

On page 10, starting on lines 18:

[Figure 7 shows] FIGS. 7a and 7b show the timing whereby signals from two devices can overlap temporarily and drive the bus at the same time.

[Figure 8 shows] FIGS. 8a and 8b show the connection and timing between bus clocks and devices on the bus.

On page 34, starting on line 4:

Slave devices do not need to detect a collision directly, but they must wait to do anything irrecoverable until the last byte (byte 5) is read to ensure that the packet is valid. A request packet with Master[0:3] equal to 0 (a retry signal) is ignored and does not cause a collision. The subsequent bytes of such a packet are ignored.

On page 40, starting on line 19:

In a preferred embodiment, a standard data block size can be selected for use with ECC, and the ECC method will determine the required number of bits of information in a corresponding ECC block. RAMs containing ECC information can be programmed to store an access time that is equal to: (1) the access time of the normal RAM (containing data) plus the time to access a standard data block (for corrected data) minus the time to send a request packet (6 bytes); [or] (2) the access time of a normal RAM minus the time to access a standard ECC block minus the time to send a request packet. To read a data block and the corresponding ECC block, the master simply issues a request for the data immediately followed by a request for the ECC block. The ECC RAM will wait for the selected access time then drive its data onto the bus right after (in case (1) above) the data RAM has finished driving out the data block. Persons skilled in the art will recognize that the access time described in case (2) above can be used to drive ECC data before the data is driven onto the bus lines and will recognize that writing data can be done by analogy with the method described for a read. Persons skilled in the art will also recognize the adjustments that must be made in the bus-busy structure and the request packet arbitration methods of this invention in order to accommodate these paired ECC requests.

On page 45, starting on line 17:

Referring to [Fig. 7] FIGS. 7a and 7b, although there is no stable condition where two devices drive the bus at the same time, conditions can arise because of propagation delay on the wires where one device, A 41, can start driving its part of the bus 44 while the bus is still being driven by another device, B 42 (already asserting a logical 1 on the bus). In a system using current drivers, when B 42 is driving the bus (before time 46), the value at points 44 and 45 is logical 1. If B 42 switches off at time 46 just when A 41 switches on, the additional drive by device A 41 causes the voltage at the output 44 of A 41 to briefly below the normal value. The voltage returns to its normal value at time 47 when the effect of device B 42 turning off is felt. The voltage at point 45 goes to logical 0 when device B 42 turns off, then drops at time 47 when the effect of device A 41 turning on is felt. Since the logical 1 driven by current from device A 41 is propagated irrespective of the previous value on the bus, the value on the bus is guaranteed to settle after one time of flight (t_f) delay, that is, the time it takes a signal to propagate from one end of the bus to the other. If a voltage drive was used (as in ECL wired-ORing), a logical 1 on the bus (from device B 42 being previously driven) would prevent the transition put out by device A 41 being felt at the most remote part of the system, e.g., device 43, until the turnoff waveform from device B 42 reached device A 41 plus one time of flight delay, giving a worst case settling time of twice the time of flight delay.

On page 46, starting on line 20:

Clocking a high speed bus accurately without introducing error due to propagation delays can be implemented by having each device monitor two bus clock signals and then derive internally a device clock, the true system clock. The bus clock information can be sent on one or two lines to provide a mechanism for each bused device to generate an internal device clock with zero skew relative to all the other device clocks. Referring to [Figure 8] FIG. 8a, in the preferred implementation, a bus clock generator 50 at one end of the bus propagates an early bus clock signal in one direction along the bus, for example on line 53 [from

left to right] from right to left, to the far end of the bus. The same clock signal then is passed through the direct connection shown to a second line 54, and returns as a late bus clock signal along the bus from the far and to the origin, propagating from [right] left to [left] right. A single bus clock line can be used if it is left unterminated at the far end of the bus, allowing the early bus clock signal to reflect back along the same line as a late bus clock signal.

On page 49, starting on line 12:

Referring to FIG. 9, each primary bus unit can be mounted on a single circuit board 66, sometimes called a memory stick. Each transceiver device 19 in turn connects to a transceiver bus 65, similar or identical in electrical and other respects to the primary bus 18 described at length above. In a preferred implementation, all masters are situated on the transceiver bus so there are no transceiver delays between masters and all memory devices are on primary bus units so that all memory accesses experience an equivalent transceiver delay, but persons skilled in the art will recognize how to implement systems which have masters on more than one bus unit and memory devices on the transceiver bus as well as on [primay] primary bus units. In general, each teaching of this invention which refers to a memory device can be practiced using a transceiver device and one or more memory devices on an attached primary bus unit. Other devices, generically referred to as peripheral devices, including disk controllers, video controllers or I/O devices can also be attached to either the transceiver bus or a primary bus unit, as desired. Persons skilled in the art will recognize how to use a single primary bus unit or multiple primary bus units as needed with a transceiver bus in certain system designs.

On page 53, starting on line 24:

A block diagram of the preferred input/output circuit for address/data/control lines is shown in FIG. 10. This circuitry is particularly well-suited for use in DRAM devices but it can be used or modified by one skilled in the art for use in other devices connected to the bus of this invention. It consists

of a set of input receivers 71, 72 and output driver 76 connected to input/output line 69 and pad 75 and circuitry to use the internal clock 73 and internal clock complement 74 to drive the input interface. The clocked input receivers take advantage of the synchronous nature of the bus. To further reduce the performance requirements for device input receivers, each device pin, and thus each bus line, is connected to two clocked receivers, one to sample the even cycle inputs, the other to sample the odd cycle inputs. By thus de-multiplexing the input [70]69 at the pin, each clocked amplifier is given a full 2 ns cycle to amplify the bus low-voltage-swing signal into a full value CMOS logic signal. Persons skilled in the art will recognize that additional clocked input receivers can be used within the teachings of this invention. For example, four input receivers could be connected to each device pin and clocked by a modified internal device clock to transfer sequential bits from the bus to internal device circuits, allowing still higher external bus speeds or still longer settling times to amplify the bus low-voltage-swing signal into a full value CMOS logic signal.

On page 58, starting on line 13:

In the preferred embodiment, two sets of these delay lines are used, one to generate the true value of the internal device clock 73, and the other to generate the complement 74 without adding any inverter delay. The dual circuit allows generation of truly complementary clocks, with extremely small skew. The complement internal device clock is used to clock the `event` input receivers to sample at time 127, while the true internal device clock is used to clock the `odd` input receivers to sample at time 125. The true and complement internal device clocks 73 and 74 are also used to select which data is driven to the output drivers. The gate delay between the internal device clock and output circuits driving the bus is slightly greater than the corresponding delay for the input circuits, which means that the new data always will be driven on the bus slightly after the old data has been sampled.

Starting on page 60, line 1:

Running the internal I/O lines in the conventional way at high bus cycle rates is not possible. In the preferred method, several (preferably 4) bytes are read or written during each cycle and the column access path is modified to run at a lower rate (the inverse of the number of bytes accessed per cycle, preferably 1/4 of the bus cycle rate). Three different techniques are used to provide the additional internal I/O lines required and to supply data to memory cells at this rate. First, the number of I/O bit lines in each subarray running through the column decoder 147 A, B is increased, for example, to 16, eight for each of the two columns of column sense amps and the column decoder selects one set of columns from the "top" half 148 of subarray 150 and one set of columns from the "bottom" half 149 during each cycle, where the column decoder selects one column sense amp per I/O bit line. Second, each column I/O line is divided into two halves, carrying data independently over separate internal I/O lines from the left half 147A and right half 147B of each subarray (dividing each subarray into quadrants) and the column decoder selects sense amps from each right and left half of the subarray, doubling the number of bits available at each cycle. Thus each column decode selection turns on n column sense amps, where n equals four (top left and right, bottom left and right quadrants) times the number of I/O lines in the bus to each subarray quadrant (8 lines each times 4=32 lines in the preferred implementation). Finally, during each RAS cycle, two different subarrays, e.g. 157 and 153, are accessed. This doubles again the available number of I/O lines containing data. Taken together, these changes increase the internal I/O bandwidth by at least a factor of 8. Four internal buses are used to route these internal I/O lines. Increasing the number of I/O lines and then splitting them in the middle greatly reduces the capacitance of each internal I/O line which in turn reduces the column access time, increasing the column access bandwidth even further.

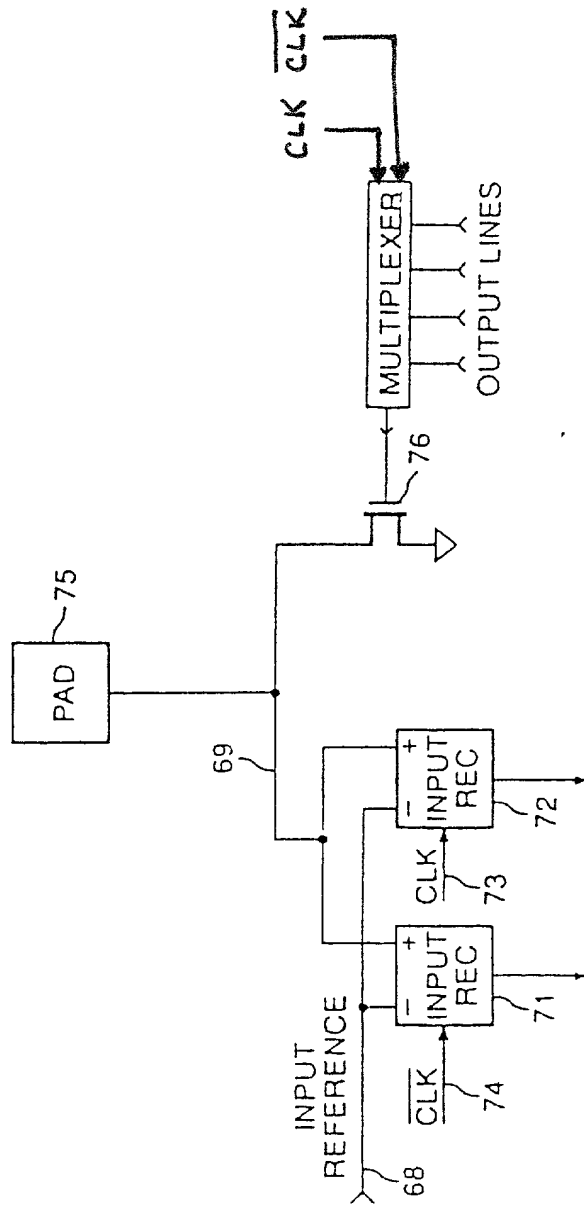


FIG. 10

